

11/4/3

Form PTO-1449 PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE CITATION (Use several sheets if necessary) Sheet 1 of <u>1</u>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">ATTORNEY DOCKET NO. <div style="font-size: 1.2em; text-align: center;">11-202</div></td> <td style="width: 50%;">SERIAL NO. <div style="font-size: 1.2em; text-align: center;">10/699831</div></td> </tr> <tr> <td colspan="2">APPLICANT <div style="text-align: center;">Kazuhiro TSURUTA</div></td> </tr> <tr> <td>FILING DATE <div style="font-size: 1.2em; text-align: center;">11/4/03</div></td> <td>GROUP</td> </tr> </table>	ATTORNEY DOCKET NO. <div style="font-size: 1.2em; text-align: center;">11-202</div>	SERIAL NO. <div style="font-size: 1.2em; text-align: center;">10/699831</div>	APPLICANT <div style="text-align: center;">Kazuhiro TSURUTA</div>		FILING DATE <div style="font-size: 1.2em; text-align: center;">11/4/03</div>	GROUP
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U.S. PATENT DOCUMENTS							
Ref. Desig.	Examiner's Initials	Document Number	Date	Name	Class/ Subclass	(If appropriate) Filing Date	
	<i>MEW</i>	4,139,442	2/13/79	Bondur et al.			
		4,238,278	12/9/80	Antipov (corres. to JP 58-37988)			
		4,910,165	3/20/90	Lee et al.			
		5,548,150	8/20/96	Omura et al.			
		5,736,749	4/7/98	Xie			
	↓	6,504,227	1/7/03	Matsuo et al. (corres. to JP 2001-77315)			

FOREIGN PATENT DOCUMENTS							
Ref. Desig.	Examiner's Initials	Document Number	Date	Country	Class/ Subclass	Translation	
						Yes	No
	<i>MEW</i>	55-78540	6/13/80	Hirobe Japan		X	
		58-37988	8/19/83	Antipov Japan			
		2001-77315 (discussed in paras 2-3 in the spec.)	3/23/01	Matsuo et al. Japan			
	↓	2001-527292	12/25/01	Erzgraber Japan		X	

OTHER DOCUMENTS (including Author, Title, Date, Pertinent Pages, etc.)		
Ref. Desig.	Examiner's Initials	
	<i>MEW</i>	"REDUCING SILICON-SUBSTRATE PARASITICS OF ON-CHIP TRANSFORMERS" by Jiang et al.; Technical Digest of The 15th IEEE International Conference on Micro Electro Mechanical Systems; 2002; pp., 649-652 (<i>discussed in page 4 of the spec.</i>)
		"FABRICATION OF THICK SILICON DIOXIDE LAYERS USING DRIE, OXIDATION AND TRENCH REFILL" by Zhang et al.; Technical Digest of The Fifteenth IEEE International Conference on Micro Electro Mechanical Systems; 2002; pp., 160-163 (<i>discussed in pgs 3-4 in the spec.</i>)
		"Large Suspended Inductors on Silicon and Their Use in a 2- m CMOS RF Amplifier" by Chang et al.; IEEE Electron Device Letters, Vol. 14, No. 5; 1993; pp., 246-248 (<i>discussed in pg. 2 of the spec.</i>)
	↓	"A Novel Buried Oxide Isolation for Monolithic RF Inductors on Silicon" by Erzgraber et al.; IEDM98-535 (1998); pp., 1-5

EXAMINER: <i>Matthew W.</i>	Date Considered: <i>4/18/05</i>
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EXAMINER: Please initial if citation considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.